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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,761	06/19/2001	Kazunobu Kuwazawa	15.44/5852	4015

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,761	KUWAZAWA, KAZUNOBU	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/25/03 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. US Patent 5,972,763 in view of Chen et al. US Patent 5,573,965 in view of Yeh et al. US Patent 5,770,508.

4. Pertaining to claims 1 and 21, Chou discloses the semiconductor method substantially as claimed. See figures 3A-3E, where Chou teaches a method for manufacturing a semiconductor device including extension regions and source/drain regions formed using a single ion-implantation step, the method comprising: (a) forming a gate dielectric layer **31** over a semiconductor substrate **30**, (b) forming a gate electrode **34** over the gate dielectric layer, (c) forming a dielectric layer **35** over the semiconductor substrate, (d) forming a mask layer **36** over the dielectric layer, (e) anisotropically etching (col., 2 lines 36-41) the mask layer to form a side

wall mask layer on sides of the gate electrode over the dielectric layer, (f) etching the dielectric layer using the side wall mask layer as a mask to form an extension control layer (extension control structures) **35a** and a side wall protection layer **37** on the sides of the gate dielectric layer (col., 2 lines 36-41), and (g) forming a first impurity layer **38** and a second impurity layer **39** by ion-implanting an impurity in the semiconductor substrate, wherein, the ion-implanting includes implanting an impurity through the extension control layer into the semiconductor substrate and the implanting also includes implanting an impurity directly into the semiconductor substrate in a region adjacent to the extension control layer; and wherein an extension region is formed in the semiconductor substrate below the extension control layer during the ion-implanting used to form the first impurity layer and the second impurity layer (see figure 3E and col. 2 lines 41-47).

5. Pertaining to claims 2 and 22, Chou teaches a method, wherein (f) further includes the step of forming a sidewall protection layer on sidewalls of the gate electrode.

6. Pertaining to claims 3 and 23, Chou teaches a method, further including removing the sidewall mask layer after the isotropic ally etching the dielectric layer and prior to the forming a first impurity layer and a second impurity layer.

7. Pertaining to claims 4, 5, 24, and 26, Chou teaches a method wherein the extension control layer is formed from a material comprising silicon and the sidewall mask layer is formed of a material comprising silicon oxide.

8. Pertaining to claim 25, Chou teaches a method wherein the ion-implanting step is carried out as a single ion-implantation operation.

9. Shown in figure 3E, and as stated in col. 2, lines 36-59, Chou teaches that the spacer **37** and the L-shaped silicon nitride layer **35a** are anisotropically etched. However, Chou fails to

show the step of (f) where etching the dielectric layer using the sidewall mask layer as a mask to form an extension control layer and a sidewall protection layer on sides of the gate dielectric layer, is etched isotropic ally. In addition, pertaining to claims 6 and 7, both Chou and Chen fail to teach wherein the extension control layer and the sidewall mask layer are formed of the materials silicon oxide and silicon nitride, in addition, there thickness of 5-50 nm and 30-200 nm, respectively. See figures 5-7, and as stated in col. 4, lines 29-30, where Chen teaches an wet-etch resistant material **22.4** such as silicon nitride where wet-etching is well know in the art to be conventionally isotropic. In addition, Pertaining to claims 6-9, see figure 2B, and as stated in col. 3, lines 40-45, where Yeh teaches that the second insulating layer **26** and the third insulating layer **28** are formed of the material of silicon dioxide and silicon nitride respectively and there specific thickness. In view of Chen it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Chen into the Chou semiconductor method because Chen teaches that a wet-etching process is performed where the wet-etch resistant material is made of silicon nitride, in addition, since Chou teaches that the L-shape spacer made of a silicon nitride material, therefore it would be obvious that the L-shape spacer made of a silicon nitride material would include an isotropic ally etched technique such as wet-etching. In view of Yeh, it would have been obvious to one of ordinary skill in the art to incorporate the materials and thickness of Yeh into the Chen and Chou semiconductor method because Yeh is specifically drawn to forming an L-shape spacer where ion-implantation techniques are performed.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
June 17, 2004

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800